Device Modeling and Applications in Silicon RF IC Design

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ABSTRACT

Recent trends in modern mobile communication systems point towards the development of silicon RF ICs. A principal issue encountered in the design of integrated RF circuits is the proper modeling of the active and passive elements in the frequency band up to 10 GHz. In this paper, the accurate modeling of active and passive devices up to several GHz is discussed. The operation of bipolar and MOS transistors at high frequencies is presented along with the effective usage of on-chip inductors and varactors. Cell design examples are provided.

I. INTRODUCTION

Modern mobile communication systems demand circuits with higher scale of integration in order to achieve smaller mobile terminal size, reduced production cost and minimal power dissipation. Commercial products operating up to 2 GHz (e.g. DECT cordless phones) successfully utilize separate integrated circuits for the RF, the IF and the baseband processing parts. However, fully integrated solutions that incorporate all three parts on a single-chip have already been proposed [1] but none of them has been adopted commercially, yet. The fundamental cells of the RF part of a transceiver are the low-noise amplifier (LNA), the power amplifier (PA) and the mixer circuits. All these cells belong to the RF front-end, which is the most power hungry among all the constituents of a communications system. The preferred technologies for its implementation are usually those that contain bipolar transistors, although several efforts have already taken place in CMOS technologies.

The bipolar transistor has two noticeable advantages over the MOS transistor: a) its transconductance for a specific amount of bias current is almost two orders of magnitude higher and b) the unity gain frequency is higher, too. Large transconductance value leads to a higher gain level with lower power dissipation, while greater unity gain frequency extends the system's operability to a higher frequency band. Three main technology categories contain bipolar transistors with different quantitative characteristics. Specifically, these technologies are the pure silicon bipolar, the BiCMOS and the Silicon-Germanium (SiGe) with heterojunction bipolar transistors (HBTs). The current trend in the fabrication of integrated circuits for RF applications is the usage of the BiCMOS technology. BiCMOS allows the coexistence of bipolar and MOS transistors on the same chip. In this case, the RF (bipolar) part is integrated with the complicated digital subsystem of the baseband signal processing (CMOS). The obvious advantage is the integration of the whole mobile system on a single silicon die. The drawback is the increased fabrication cost of BiCMOS and the worse bipolar transistor performance compared to those of a pure high-speed bipolar technology. As an example, the unity gain frequency of a bipolar transistor in a pure bipolar technology is as much as double of that of a bipolar transistor in a BiCMOS technology. The relatively novel SiGe HBT technology can lead to the design of analog RF and digital subsystems to even higher frequency ranges. However, its main disadvantage is the increase of the fabrication cost.

On the other side, the continuous improvement of CMOS technologies and particularly the reduction of the channel dimensions of the MOS transistor (submicron technologies) gradually makes MOS transistors as fast as bipolar ones. Moreover, MOS transistors exhibit much lower noise levels and better linearity. It is possible that shortly, when CMOS technology reaches 0.1μm, the full integration of a mobile communications system in CMOS technology will be feasible since MOS transistor unity gain frequency will significantly increase.

Apart from active elements in RF IC design, recently, it has been proven that the successful usage of passive elements such as on-chip spiral inductors and varactors is feasible through proper device modeling. In the past, the lack of a proper modeling technique kept designers reluctant to incorporate passive elements in their designs, especially spiral inductors. However, generic and process independent models have been reported in literature that can handle any polygonal-shape as well as multi-layer inductors [2]-[3].

II. TRANSISTOR MODELING

A. Bipolar Transistors

The bipolar transistor is the active device most frequently used in silicon RF IC design. Detailed knowledge of the geometry of the device and how it affects its electrical behavior is mandatory to the high-frequency IC designer. For example, in many cases, a high transconductance value is demanded for proper circuit operation. This can be accomplished by simply increasing the geometrical dimensions of the transistor which on the other hand leads to an increase of the parasitic capacitances between base and emitter, collector and

base and, base and substrate. This dependence must be taken into account in the design of the final circuit and specifically, in the frequency response evaluation.

The basic parameters of the electrical behavior of the bipolar transistor that are directly related to its geometry, are:

- The saturation current I_S. This parameter is directly related to the transconductance of the device.
- The base resistance, r_b. The base resistance is a crucial parameter that strongly affects the noise performance.
- The collector resistance r_c. The evaluation of this resistance is quite complicated due to the physical construction of the collector area of the bipolar transistor. Special layers have been developed to reduce its value.
- The parasitic capacitances of the device (C_{je}, C_μ and, C_{cs}) along with the base transit-time, define the frequency profile of the transistor.

The parasitic resistances and the parasitic capacitances of the bipolar transistor vary oppositely with respect to the geometrical dimensions of the device, so a compromise must be considered depending on the specifications of the circuit under development.

B. MOS Transistors

The recent advances in CMOS technologies have made possible the introduction of the MOS device in silicon RF IC designs. The benefits from the usage of MOS technology are obvious: higher level of integration due to its compatibility with the baseband signal processing part, and cost reduction. The major obstacles here are the lower g_m/I_D ratio and cutoff frequency with respect to the bipolar counterparts, as well as poor device modeling. A lot of effort has been dedicated in the past years towards the development of robust MOS transistor simulation models for analog work and benchmark tests have been proposed [4] to test the validity of existing ones. Moreover, operation at high frequencies introduces extra problems in the prediction of the device's behavior. A figure-of-merit here is the so-called *intrinsic cutoff frequency* of the transistor, defined as follows:

$$f_{Ti} \cong \frac{3}{2}\frac{\mu(V_{GS}-V_T)}{2\pi(1+\delta)L^2} \quad (1)$$

where μ is the carrier mobility, V_T is the threshold voltage, δ ranges between 0 and 1 and L is the channel length.

The frequency range of validity of each transistor model is defined against the above-defined frequency. For example, the basic quasi-static model [5] is valid up to the 1/10 of f_{Ti} and the more detailed model that includes transcapacitances is valid up to the 1/3 of f_{Ti}. At very high frequencies of operation, the gate charge cannot follow the voltage signal variation any more and thus, a phase lag is introduced. This effect is taken into account in non-quasi-static models by replacing the transistor's transconductance g_m by a transadmittance y_m. A simple non-quasi-static model has been recently introduced in the BSIM3v3.1 MOS transistor model; this model is valid up to frequency f_{Ti} [6].

Another important factor, when operating at high frequencies, is the noise performance of the MOS transistor. Here, the major noise source is the channel's thermal noise. However, additional noise sources are revealed including the gate's distributed thermal noise and the induced current noise at the gate [7]. The latter is defined by:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_{gs} \quad (2)$$

where

$$g_{gs} = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (3)$$

From the above equations, it is obvious that the gate induced current noise is proportional to ω^2, a fact that must be seriously taken into account when operating at high frequencies.

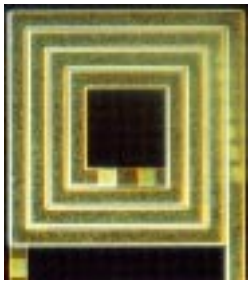
From a process technology point of view, the major effort is focused on the minimization of transistor's channel length in order to increase the level of integration and the minimization of oxide thickness to increase the transconductance. However, this leads to more noisy devices and thus there is a limit in devices' dimensions if they are to be used in high frequency applications: 0.25 μm CMOS technology seems to be the limit for safe and robust HF circuit designs.

III. PASSIVE ELEMENTS

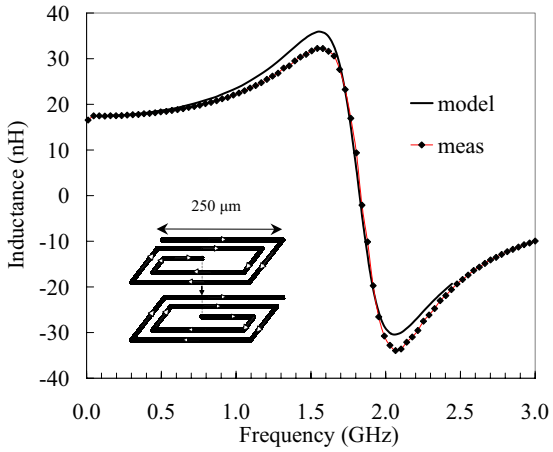
A. On-chip Spiral Inductors

On-chip inductors generally enhance the reliability and efficiency of silicon integrated RF cells; they offer circuit solutions with superior noise performance and contribute to a high level of integration. However, poor integrated inductor modeling has been so far a major obstacle in their extensive utilization. In order to overcome this problem, a complete modeling and CAD tool, called "SISP" (Spiral Inductor Simulation Program), has been developed [2]-[3]. Polygonal and multi-layer integrated inductors, as well as transformers on silicon substrates can be accurately modeled up to several gigahertz. The model is generic in terms of geometry and technology. It comprises lumped elements in a SPICE subcircuit format and requires no further adjustment after fabrication and measurement. Therefore, the designer can avoid any extra fabrication cycle. Calculation of inductance and quality factor versus frequency is feasible even beyond first resonance. As an example, in Fig. 1(b) the accurate prediction of the inductance and the self-resonance frequency of a square two-layer inductor [3] is displayed (Fig. 1(a)). Another substantial feature of SISP is the precise modeling of the coupling among two or more on-chip inductors [3].

The current trend in 1-2GHz one-chip RF front-ends dictates the existence of more than one inductor on the same chip [8], [9], [10].



(a)



(b)

Fig. 1. (a) Two-layer inductor microphotograph (250µm x 250µm)
(b) Modeled and measured inductance [31]

In this case, the magnetic coupling between individual inductors or in intended transformers can play an important role in the performance of the overall system. Therefore, the layout of the circuit drastically affects the electrical behavior. SISP is capable of predicting related phenomena, leading to reliable and effective SPICE simulations and thus drastically reducing design effort.

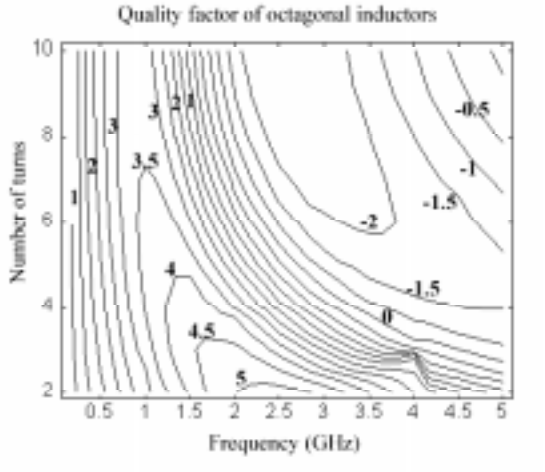


Fig. 2. Quality factor of octagonal spiral inductors with radius of 200µm, track width of 14µm and spacing between tracks of 3µm

The software tool can also be proven useful in optimizing the performance of integrated inductors by modifying their geometrical characteristics i.e. number of turns, segment width, segment distance, etc. As an example, octagonal spiral inductors in a three-metal layer digital CMOS process were modeled and simulated to demonstrate how the quality factor (Q) depends on the number of turns and the operating frequency. Simulation results are summarized in the form of a nomograph displayed in Fig. 2.

B. Varactors

Varactors are devices with tunable capacitance (Fig. 3(a)). They are typically implemented as p-n junctions in

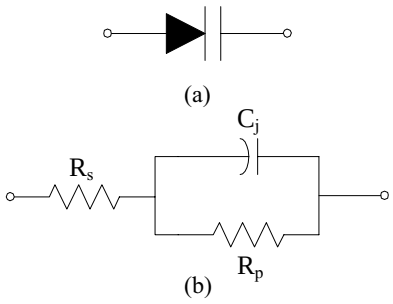


Fig. 3. (a) Varactor symbol (b) Equivalent varactor model

integrated silicon technologies. Fig. 3(b) displays a simple varactor diode model. C_j is the junction capacitance, R_p is the equivalent resistance of the recombination procedure and surface leakage current, and R_s is the series parasitic resistance. The quality factor of a varactor is given by (4):

$$Q \cong \frac{\omega C_j R_p}{1 + \omega^2 C_j^2 R_p R_s} \tag{4}$$

The quality factor is a very essential parameter in the design of integrated voltage-controlled oscillators (VCOs). Combined with the quality factor of the integrated inductor used, it can tune the performance of the circuit, especially the phase noise. At low frequencies, resistance R_p plays an important role in the varactor's quality, while at high frequencies R_s dominates. As a result, the quality factor at a frequency greater than a few MHz is given [11] by (5):

$$Q \cong \frac{1}{\omega R_s C_j} \tag{5}$$

Quality factor increases as the inverse bias increases. However, the phenomenon is constrained by the breakdown voltage of the junction diode.

In a bipolar technology for RF applications, a varactor is formed by the p-n junction between the collector and the base part of a bipolar transistor. In a CMOS technology the varactor is formed by the p-n junction between the p-type substrate and n+ implantation or the n-type well and the p+ implantation.

IV. RF CELL EXAMPLES

A. Low-Noise Amplifiers

The Low-Noise Amplifier is one of the most important parts of a telecommunications transceiver. It is the first active cell of the receiver part following the antenna and thus, its performance drastically affects the noise

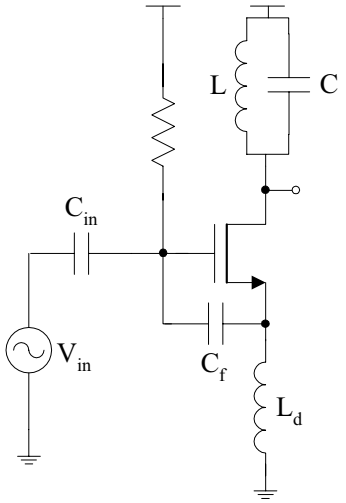


Fig. 4. Tuned amplifier

level of the system as well as its input voltage standing wave ratio. Therefore, the LNA must exhibit low noise figure, high gain, high linearity and good input impedance matching. Various implementations of integrated silicon LNAs operating up to 2 GHz have been recently reported in the literature. These include bipolar [12], BiCMOS [13] and, CMOS [14] implementations.

A special class of low-noise amplifiers in telecommunication receivers is the tuned amplifier. The implementation of such circuits demands apart from fast active elements, high-quality passive devices such as integrated inductors and capacitors. The simplified schematic of a MOS tuned amplifier is shown in Fig. 4. As can be seen from the figure, more than one integrated inductor is used in the design. In this case, the magnetic coupling between them can seriously affect the overall performance of the circuit and thus, it must be taken into account. The previously mentioned software (SISP) can be used in the evaluation of the magnetic coupling with respect to the placement of the inductive devices and thus, the electrical performance versus occupied silicon area can be optimized.

The LC parallel resonance circuit used as a load in the tuned amplifier cell can be simply implemented using only one device, namely, the integrated inductor. There is no need to have a separate capacitor on-chip since the parasitic capacitance of the integrated inductor to the substrate can be used as a substitute. For this purpose, the inductive device is designed in such a way that its first self-resonance frequency falls in the frequency band of interest for the operation of the tuned amplifier. Again, SISP can be used for the proper design of the device.

A second version of the proposed topology in Fig. 4 is shown in Fig. 5 [1]. Here, the amplifier is fully balanced and the two RF input signals are usually provided externally through a balun. Some attempts have been reported to internally design the baluns using integrated inductors but the process quality is very critical in the proper implementation of such a device.

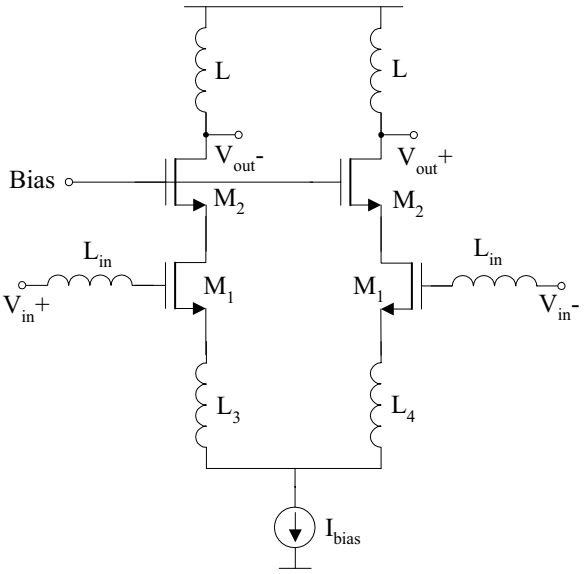


Fig. 5. Fully balanced low-noise amplifier

B. Integrated Continuous-Time RF Filters

Continuous-time filters are indispensable parts of any RF front-end. Fig. 6 shows the typical architecture of the receive path of a RF front-end. A bandpass filter precedes the LNA and provides channel pre-selection and suppression of unwanted signals. An image-rejection

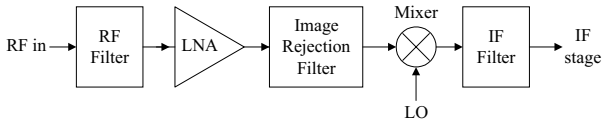


Fig. 6. RF receiver front-end

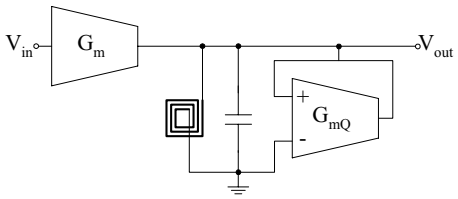


Fig. 7. Active RLC filter

filter (band-pass or notch type) follows the LNA and contributes to the rejection of the image frequencies that overlap with the desired RF signal after mixing. Further IF filtering (low-pass) may be needed to discard high order products at the mixer output.

Traditionally, RF filters have been implemented as off-chip passive devices, using such technologies as Surface-Acoustic-Wave (SAW) and ceramic. Putting filters on the same chip with the rest of the RF cells is of particularly great interest: it would lead to a higher level of integration and reduce the number of off-chip excursions that require matching and are a major source of power dissipation. Furthermore, active filter schemes offer programmability, which is a boon, especially when designing multi-mode transceivers. To this extent, several attempts have been made to integrate active RF filters; references [15] to [22] present some of the most

interesting ones, with emphasis on silicon bipolar and CMOS implementations [15]-[20].

Passive components are used extensively in most integrated RF filter designs. On-chip inductors and capacitors form tuned elements for band-pass filters [15]-[22]. Varactors are used for frequency adjusting tuned elements [21], [22]. The precise modeling of the properties and tolerances associated with passive components can shorten the filter design cycle and lead to chips optimized for area and power.

In [8], a 1.8 GHz band-pass filter with tunable center frequency and quality factor was presented. The main idea is shown in Fig. 7. A transconductor (*Gm*) drives an on-chip LC tank. Another transconductor (Gm_Q) connected as a negative resistance provides Q-enhancement, compensating for the finite Qs of the capacitor and the inductor. This work proved the feasibility of integrating RF filters for telecommunication applications. However, in order to meet strigent tranceiver specifications, improved dynamic range and noise performance, as well as on-chip automatic tuning schemes remain to be addressed.

V. CONCLUSIONS

In this paper, current trends in RF IC design were presented. Extensive usage of silicon technologies increases the integration level and reduces cost and power dissipation. However, poor device modeling (both active and passive) is a major obstacle towards this target. Certain issues such as frequency range of validity of the MOS transistor and integrated inductor modeling are addressed and solutions are outlined. Finally, the above approaches are introduced in the design of integrated RF cells, such as LNAs and RF filters.

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