EFFICIENT UTILIZATION OF ON-CHIP INDUCTORS IN SILICON RF IC DESIGN USING A NOVEL CAD TOOL; THE LNA PARADIGM

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***Abstract*—A CAD tool for modeling planar and multi-layer polygonal integrated inductors on silicon substrates has been developed. The tool can be used in the efficient design of RF ICs containing on-chip inductors. The accuracy and reliability of the software is established through measurement results. The CAD tool is then used in the extraction of design guidelines for the development of inductor structures suitable for a given application. This procedure is demonstrated with the design of an LNA.**

I. INTRODUCTION

The recent boom in portable wireless communications applications in combination with the advances in silicon technology make the implementation of silicon RF front-end ICs operating in the low GHz range both technically and economically attractive.

On-chip inductors generally enhance the reliability and efficiency of silicon integrated RF cells; they offer circuit solutions with superior noise performance and contribute to a high level of integration. However, poor integrated inductor modeling has been so far a major obstacle in their extensive utilization. In order to overcome this problem, a complete modeling and CAD tool, called "SISP" (Spiral Inductor Simulation Program), has been developed and presented in [1][2]. Polygonal and multi-layer integrated inductors, as well as transformers on silicon substrates can be accurately modeled up to several gigahertz. As an example, in Fig. 1(b) the accurate prediction of the inductance and the self-resonance frequency of a square two-layer inductor (Fig. 1(a)) is displayed [2]. Another substantial feature of SISP is the precise modeling of the coupling among two or more on-chip inductors [2].

In this paper, the utilization of the above features of the software for the successful exploitation of integrated inductors in silicon RF IC designs will be demonstrated. In section II a brief presentation of SISP's features will be shown, followed by a comparison between measurement and simulation results. Section III contains useful integrated inductor design guidelines in the form of comprehensive nomographs. Section IV presents a design example employing SISP, and in particular a low noise amplifier operating in the vicinity of 1 GHz. Finally, section V contains the conclusions.

II. SISP: A BRIEF PRESENTATION

Spiral Inductor Simulation Program is a PC-based CAD program developed in C++. The core algorithm, which has been analytically presented in [1], extracts a two-port network consisting of eleven lumped elements for every segment of the inductor. The main elements of the two-port are the series

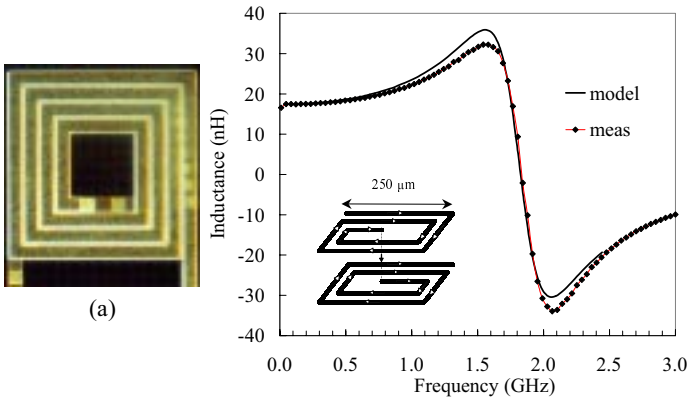

Fig. 1. (a) Two-layer inductor microphotograph (250µm x 250µm) (b) Modeled and measured inductance [2]

inductance, the resistance of the segment and the capacitors formed by the insulating SiO_2 between the inductor and the Si substrate. The algorithm also calculates the coupling capacitances between parallel adjacent segments and the RC networks for the modeling of the substrate layers under the insulator. The mutual inductance between the segments of the spiral is modeled with a transformer. The equivalent circuit of the spiral inductor includes a transformer for every possible couple of segments. The feature that enhances the accuracy of the inductor model, above the first resonance frequency, is the utilization of a full capacitance matrix. The matrix contains a capacitor not only between adjacent segments but also for every possible pair of segments of the inductor. This improvement is currently being added to the core algorithm of SISP employing techniques presented in [3].

SISP's layout tool can generate spiral inductor structures or alternatively import layout designs in CIF format. The designer should enter the CMOS, BiCMOS or bipolar process parameters before creating a layout. A fast, segment by segment extraction of the equivalent SPICE subcircuit is executed within seconds, while a similar model extraction with any EM software would take days. Three distinct versions of the model are produced to accommodate "typical", "fast" and "slow" technology variations. Passive elements may be frequency dependent to incorporate conductor skin effect, if supported by the SPICE simulator being used. Simulations can be initiated through the user-interface. The software displays simulation results in rectangular, polar or Smith chart plots, against measurement results (from S-parameter sets), if any. As an example, Fig. 2 displays the comparison between measurement and simulation results of a 12-turn octagonal inductor fabricated in a typical silicon bipolar process.

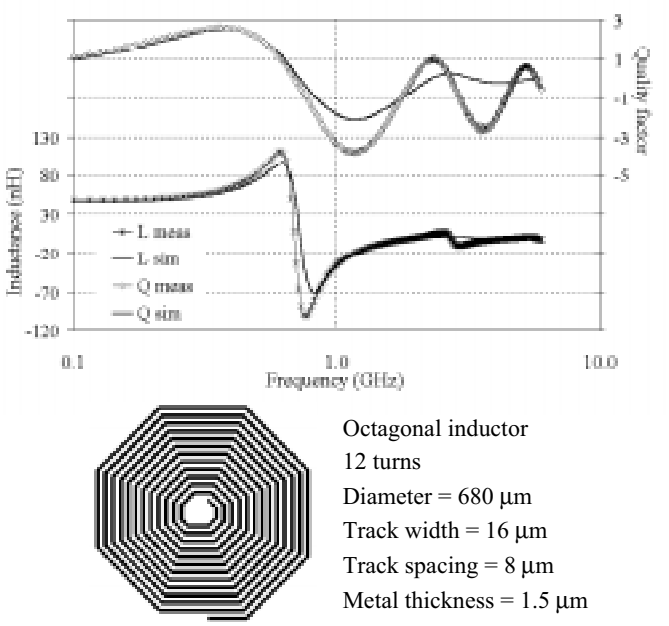

Fig. 2. Simulation vs. measurement of an octagonal inductor

III. INDUCTOR OPTIMIZATION GUIDELINES

Having already established the reliability of the SISP software [1][2], the tool can be used in the performance optimization of on-chip inductors. This can be done in two ways: (a) by optimizing the geometrical characteristics (i.e. number of turns, segment width, segment distance, etc.) of the spiral inductors, and (b) by deriving hints for process modifications, if supported by the foundry. The ease of use and speed of operation of the SISP software allows the generation of the useful nomographs that can prove to be a valuable aid to the RF IC designer in order to optimize his/her circuits. Various RF applications increasingly demand the improvement of the performance of on-chip inductors beyond the current state-of-the-art. Towards this purpose, modifications of certain parameters of a silicon process, such as Al metalization thickness and substrate doping, may be imperative [4].

Octagonal spiral inductors in a three-metal layer digital CMOS process were modeled and simulated to demonstrate how the quality factor (Q) and the inductance (L) depend on the number of turns. Simulation results are summarized in the form of nomographs. Fig. 3 displays the Q and Fig. 4 the L of octagonal inductors with a radius of 200μm, versus frequency and number of turns. From these nomographs, the highest values of L and Q and the respective resonance frequencies are found, while silicon area remains constant and the number of turns varies. Furthermore, Fig. 5 presents the improvement in the quality factor of a square inductor while the thickness of the metal track increases. Important is the fact that the resonance frequency of this family of inductors remains almost constant for the specific range of heights. In similar ways, nomographs can reveal the direction towards which technology parameters should be altered.

IV. THE LNA PARADIGM

The current trend in 1-2GHz one-chip RF front-ends dictates the existence of more than one inductor on the same chip ([5], [6], [7]). In this case, the magnetic coupling between individual inductors or in intended transformers can play an important role in the performance of the overall system. Therefore, the layout of the circuit drastically affects its electrical behavior.

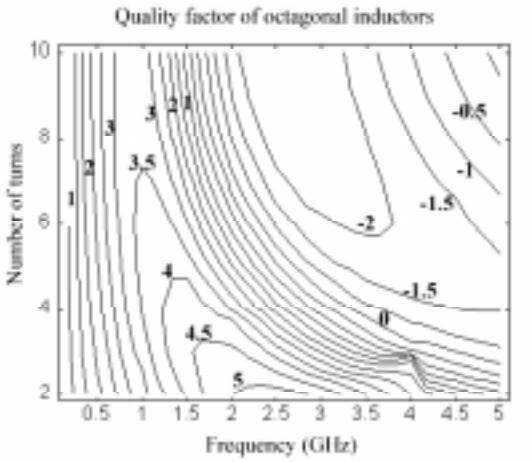

Fig. 3. Quality factor of octagonal spiral inductors with radius of 200μm, track width of 14μm and spacing between tracks of 3μm

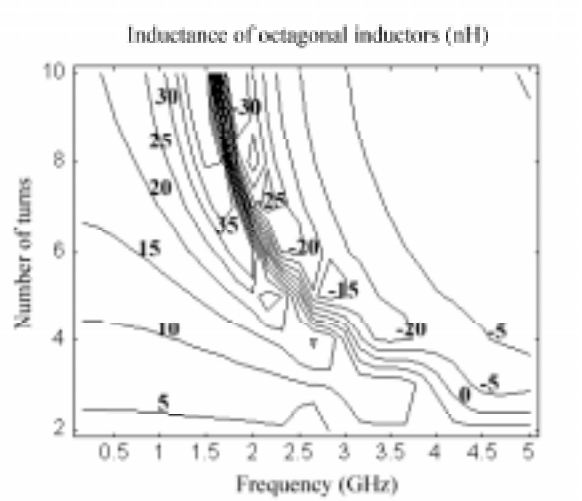

Fig. 4. Inductance of octagonal spiral inductors with radius of 200μm, track width of 14μm and spacing between tracks

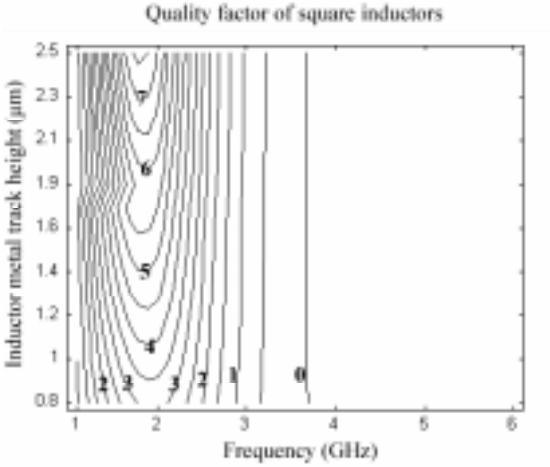

Fig. 5. Quality factor of 5-turn square spiral inductors with outer dimension of 300μm, track width of 14μm and spacing between tracks of 3μm

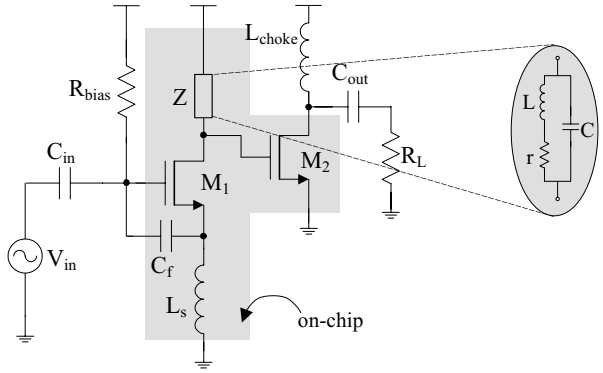

Fig. 6. LNA schematic and simplified model of the LC-tank Z

SISP is capable of predicting related phenomena, leading to reliable and effective SPICE simulations and thus drastically reducing the design effort.

In this paper, the design of a simple tuned low-noise amplifier is presented. The particular design is by no means optimized in terms of noise, gain and silicon area, but it is rather used as a vehicle to demonstrate the software's capabilities. The LNA is designed in a digital sub-micron CMOS process and is operated around 1GHz. The schematic diagram of the LNA is shown in Fig. 6, where the shaded area represents the on-chip components including load Z, that is the LC tank, and L_s, which is impedance matching inductor. The designer can select the inductors' geometry either by using nomographs or by simulation with SISP.

Using the simplified model shown in Fig. 6 for the LC tank, the gain of the LNA is given by

$$\text{Gain} = \frac{g_m + jQg_m}{r[(g_d r - \omega^2 LC + 1) + j\omega(rC + g_d L)]} \qquad (1)$$

where $Q=\omega L/r$ is the quality factor of the inductor.

It is evident that the quality factor of the inductor (defined mainly by the inductor's series resistance), strongly affects the frequency response of the LNA. Moreover, the gain of the amplifier is optimized if the value of the parallel capacitor C of the load is minimized. For this purpose, operation of the integrated inductor around its self-resonance frequency was chosen in order to eliminate the need for a capacitive element in the tank. This can be done thanks to the ability of SISP to accurately predict the inductor's behavior at high frequencies, even beyond self-resonance frequency, as it has already been shown in Fig. 1 and Fig. 2. Fig. 7 displays the inductance and quality factor of the selected 6-turn square spiral inductor versus frequency. Its outer dimensions are 470μm x 470 μm, the track width is 25μm and the spacing between the tracks is 3μm. The inductor is laid out on the third metal layer of the process.

The on-chip inductor L_s (3-turn square, 470μm x 470 μm) is used in combination with the $C_{gs}//C_f$ capacitor for 50Ω input

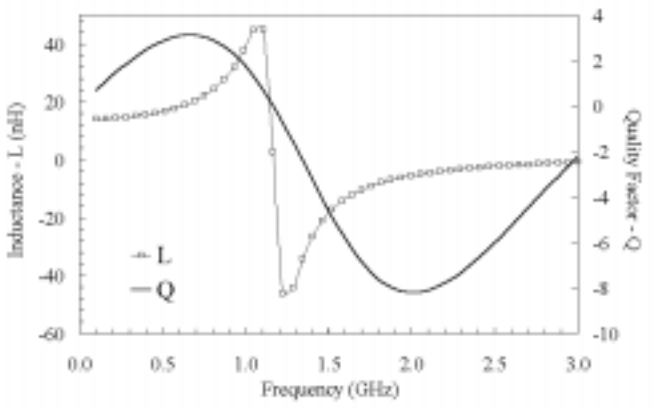

Fig. 7. Inductance and quality factor of the Z load of the LNA

matching of the LNA. The input impedance of the LNA is calculated by

$$Z_{in} = \frac{1}{sC_{gst}} + sL_s + \frac{g_m L_s}{C_{gst}} \qquad (2)$$

where $C_{gst}=C_{gs}//C_f$.

The 50Ω driving capability of the LNA is achieved through an open-drain configuration formed by transistor M_2 as shown in Fig. 6. This open-drain stage lowers the output impedance of the LNA and provides the necessary current to drive a 50Ω instrument port only for measurement purposes. Its gain does not exceed zero dB. For an integrated LNA that is used as a cell in bigger silicon RF system, the open-drain stage would not be used.

The alternative to the above input impedance matching topology is to employ an inductance L_g at the gate of the transistor M_1 as shown in Fig. 8. In this case L_g is used to cancel out the imaginary part of the input impedance caused by the parasitic capacitance C_{gs} of the device M_1. The overall input impedance is given by

$$Z_{in} = s(L_g + L_{bond}) + \frac{1}{sC_{gs}} + \frac{g_m L_{bond}}{C_{gs}} \qquad (3)$$

However, this solution has certain drawbacks: (a) the value of the inductor L_g is usually higher than that of L_s in Fig. 6, resulting in larger silicon area and (b) the impedance matching is not so broadband. The value of L_g can be reduced by employing the grounded capacitance C_g connected to the gate of M1, but this decreases the quality factor of the tuned amplifier.

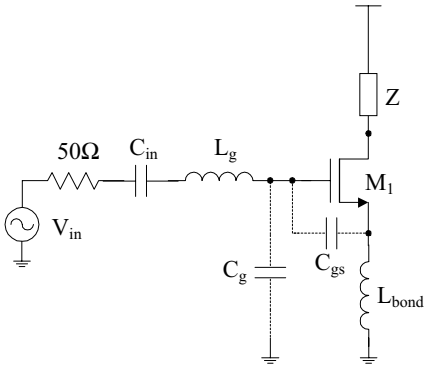

Fig. 8. Alternative input impedance matching topology

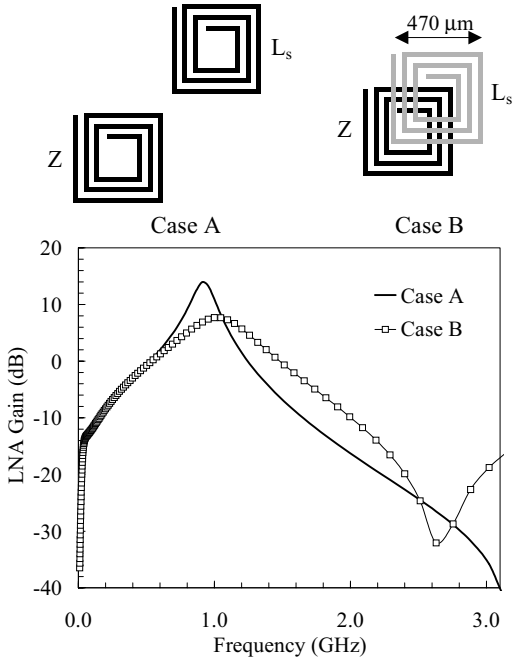

Fig. 9. LNA gain variance for two placement schemes of on-chip inductors

On-chip inductors' coupling effects

The magnetic coupling of the two integrated inductors of the LNA can seriously affect system performance and its improper modeling can lead to a degraded frequency response. Input impedance matching of the amplifier is also affected by the coupling of the two inductors. Fig. 9 depicts the LNA performance variance in terms of gain, under different inductor placement schemes, as predicted by SISP. In case A the two inductors are laid out on the third metalization layer; in case B L_s is laid out on the second layer and partly under the inductor of load Z. The diagonal placement of the devices provides the necessary magnetic isolation for the optimum operation of the amplifier, at the cost of increased area coverage. However, if the gain degradation is acceptable, case B can lead to a more compact layout. These two versions of the layout of the LNA have been submitted for fabrication.

To give a more illustrative example of how the performance of an inductor is affected by the presence of other inductors in its vicinity, Fig. 10 and Fig. 11 present the L and the Q values of a square inductor (Z) in two distinct cases as depicted in Fig. 9. Inductor L_s is driven with a separate current source that has the same phase as the source that drives Z. When L_s is too close to Z, its performance can be relatively changed, due to the magnetic coupling between the two, providing a very simple tuning tool. In other words, the L and Q values of an inductor can be tuned by varying the current of a second inductor in its vicinity.

V. CONCLUSIONS

An effective method of utilizing on-chip inductors in silicon RF IC design is demonstrated through an LNA paradigm. A novel CAD tool, SISP, is capable of modeling the coupling between adjacent spiral inductors in any metal layer, and predicting the inductor-related performance variance of RF circuits.

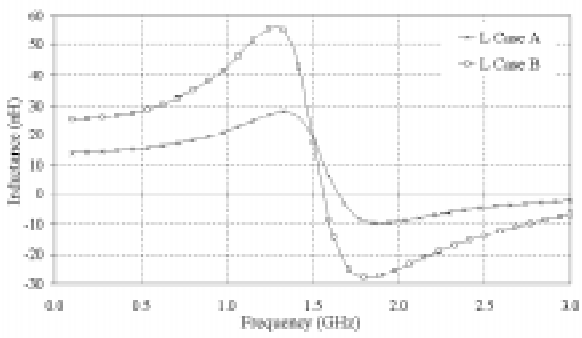

Fig. 10. Inductance of Z that is magnetically coupled to L_s

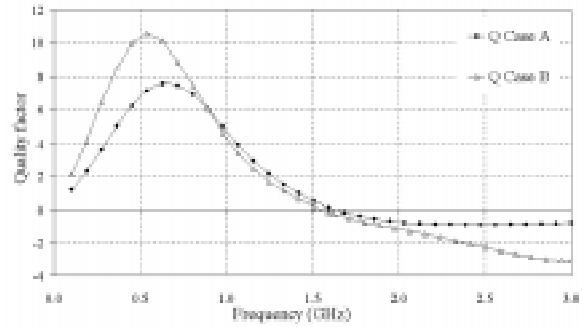

Fig. 11. Quality factor of Z that is magnetically coupled to L_s

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