SISP: A CAD TOOL FOR SIMULATING THE PERFORMANCE OF POLYGONAL AND MULTI-LAYER INTEGRATED INDUCTORS ON SILICON SUBSTRATES

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Abstract

A CAD tool for the modeling of planar and multi-layer polygonal integrated inductors on silicon substrates, is presented. The algorithm extracts a complete lumped element model for all the inductors existing on a common substrate. Octagonal, square and two-layer inductors have been designed and fabricated in three different silicon processes. Experimental results confirm the accuracy of the model, not only for a single inductor but also for two square inductors on the same silicon substrate that are magnetically coupled.

Introduction

Recently reported RF ICs (e.g. [2]) exhibit an increasing trend to incorporate integrated inductors, aiming to better performance and a higher level of integration. However, the lack of an accurate and generic model of monolithic inductors on silicon substrates has often prevented designers from employing them. In this paper, SISP, a CAD tool that generates a generic and process-independent inductor model, is presented. The properties of any inductor structure laid out on silicon and in any process can be accurately modeled. The extracted model comprises lumped elements in a SPICE subcircuit format and requires no further adjustment after fabrication and measurement. Therefore, the designer can avoid any extra fabrication cycle. Calculation of inductance and quality factor versus frequency is feasible even beyond first resonance. SISP, furthermore, computes the magnetic coupling among two or more adjacent spiral inductors of any polygonal shape. Experimental results confirm the accuracy of this modeling technique from a few megahertz up to several gigahertz.

The computer algorithm is integrated with a graphical user interface (Fig. 1) to help the designer create the layout of spiral inductors, initiate simulation and plot the results in various ways.

Several inductor structures have been fabricated and measured in three different silicon processes. Comparisons between measurement and simulation results from SISP, which are presented for a two-layer inductor and an octagonal one, establish its accuracy. Equally important is the accurate prediction of the coupling between two adjacent square spiral inductors.

SISP: A Brief Overview

Spiral Inductor Simulation Program (SISP) is a PC-based CAD program developed in C++. The core algorithm, that has been analytically presented in [1], extracts a

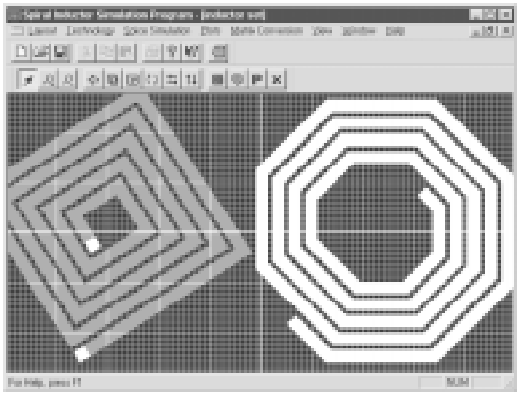

Fig. 1. SISP (Spiral Inductor Simulation Program) - Layout Editor

two-port network consisting of lumped elements, segment by segment. The electrical equivalent of the segment two-port is shown in Fig. 2. Basic steps of the algorithmic process are presented in Fig. 3. The main elements of the two-port are the series inductance L, the resistance R of the

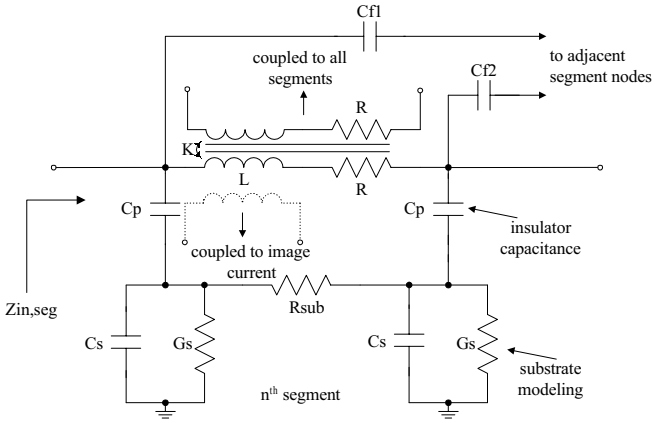

Fig. 2. Equivalent two-port for one segment of the spiral inductor.

segment and the capacitors C_p formed by the insulating SiO_2 between the inductor and the Si substrate. The algorithm also calculates the coupling capacitances C_f between parallel adjacent segments and the two elements modeling the substrate layers under the insulator namely, C_s and G_s.

The mutual inductance *M* between the segments of the spiral is modeled with a transformer. The equivalent circuit of the spiral inductor includes a transformer for every possible couple of segments. SISP contains a layout tool that can generate common spiral inductor structures or import ready-made layout designs in CIF format. The first and important step in the design sequence is the entry of the technology parameters. The designer can enter CMOS, BiCMOS or bipolar process parameters before creating the layout. A fast, segment by segment, extraction of the equivalent SPICE subcircuit can be done within seconds, while a similar model extraction with any EM software would take even days. Three distinct versions of the model can handle typical, "fast" and "slow" technology variations. Passive elements may be frequency dependent to

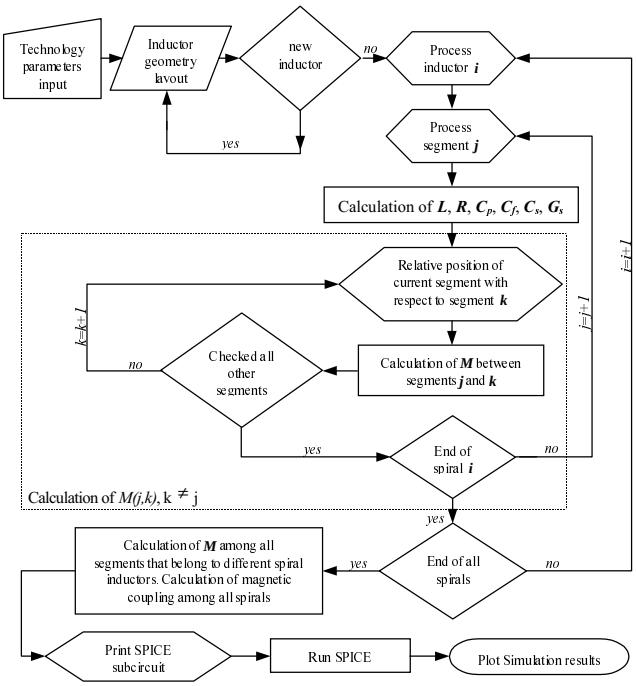

Fig. 3. Proposed algorithm for the SPICE model generation

incorporate conductor skin effect depending on the SPICE simulator being used. Simulations can be initiated through the user-interface. Finally, measurement and simulation results of S-parameters, inductance and quality factor can be combined in single plot in rectangular, in polar coordinates, or in a Smith chart.

Experimental Results - Comparisons with SISP predictions

More than twenty different spiral inductor structures have been fabricated and measured in three different silicon processes (SGS-THOMSON's bipolar HSB, ATMEL-ES2's digital CMOS ECAT05 and SIEMENS' bipolar B6HF). Three distinct cases from the above structures are presented. A two-layer inductor formed by two planar ones on different metal layers, one over the other, is shown in

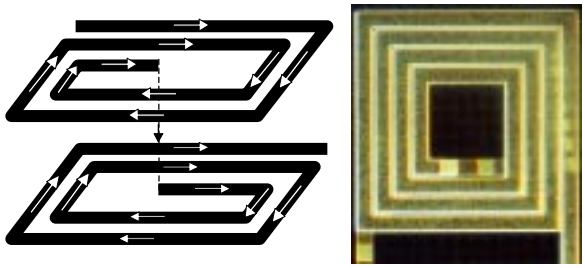

Fig. 4. Two-layer inductor: (a) current flow, (b) microphotograph.

Fig. 4(a). Due to the magnetic coupling between the two spirals, there is an increase in inductance by a factor of five compared to the inductance of a single planar inductor,

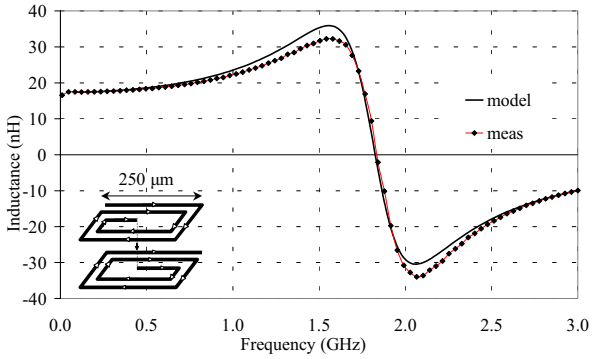

Fig. 5. Inductance of a two-layer inductor (m3-m1) with outer dimension 250μm and 4 turns.

while the quality factor remains at the same level. In Fig. 5 a comparison between the modeled and the measured inductance of a two-layer inductor (metal3-metal1, ES2-CMOS 0.5 μm) is shown. Attention should be paid to the accurate prediction of resonance and beyond even with typical process parameters. This tool is extremely valuable when the inductor is to be used, for example, as a LC-load in a tuned amplifier. The model presented above can accurately predict the tuning frequency of such an amplifier and the designer has no longer to wait until the actual measurement of the circuit. In Fig. 6, the equivalent S-parameters of the two-layer inductor are also displayed.

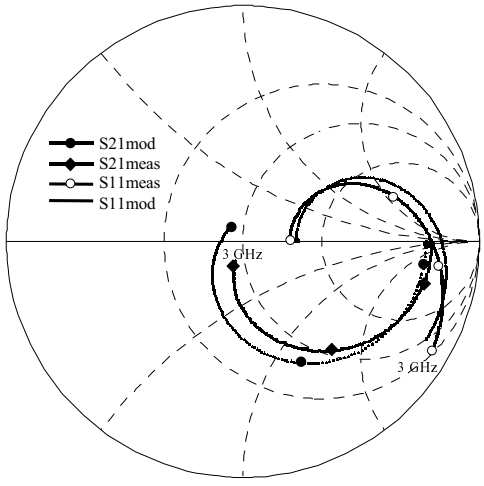

Fig. 6. S11 and S21 of the two-layer inductor.

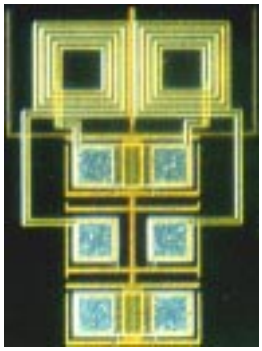

Fig. 7. Adjacent square spiral inductors. Outer dimension = 250 µm

Another important feature of SISP is the accurate modeling of the coupling between spiral inductors. A test structure fabricated by ES2 is shown in Fig. 7. Two adjacent planar square inductors were measured and modeled and the results are shown in Fig. 8. The magnetic coupling modeling enables designers to use two or more integrated inductor in RF ICs and accurately model their performance prior to fabrication.

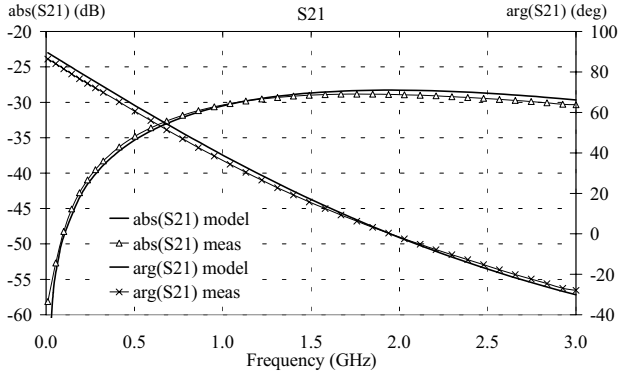

Fig. 8. Modeled and measured S21 for two adjacent square inductors.

Finally, the comparisons for the inductance and the quality factor of an 8.5-turn octagonal inductor fabricated by ST are presented in Fig. 9.

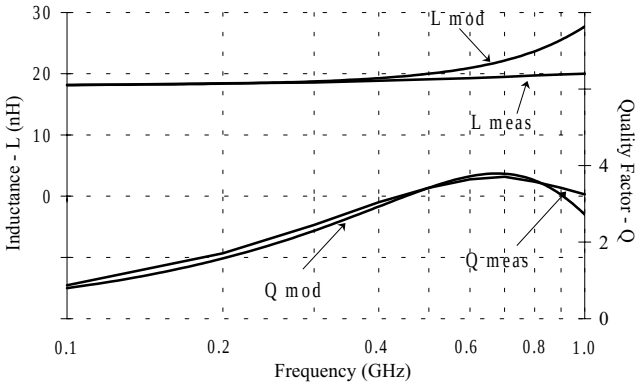

Fig. 9. Experimental results of an 8.5-turn octagonal spiral inductor

SISP as a powerful design aid

Having proven the efficiency, accuracy and generic nature of our inductor simulation tool, it can now be used as a powerful design aid for the optimization of the usage of integrated inductors in silicon RF IC designs. In Fig. 10 two nomographs developed with SISP are presented. In these nomographs, the L and Q values of a square inductor as functions of inductor turns and trach width are plotted. Such families of curves can be easily produced with SISP and help the RF IC designer to properly select the inductor that best fits his needs. Another important feature of SISP, is its ability to accurately predict the magnetic coupling between two or more inductors, thus helping the design of a robust floorplanning of the circuit

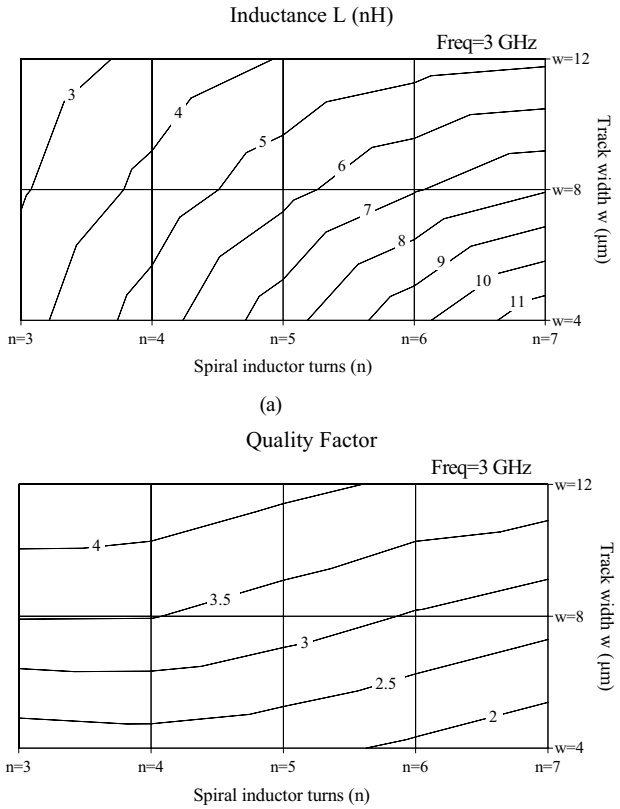

Fig. 10. (a) Inductance and (b) quality factor of square inductors with outer dimension D_0=250µm and s=3µm versus track width w and number of turns n.

Conclusions

A concrete and generic CAD tool for the analysis and design of integrated spiral inductors on silicon substrates has been presented. Comparisons with measurements have exhibited the accuracy of the modeling technique of polygonal and multi-layer inductors. The tool enables the designer to safely analyze the geometry, the type and the positioning of all the inductors in a single RF IC prior to fabrication.

References

[1] Y. Koutsoyannopoulos, Y. Papananos, C. Alemanni, S. Bantas, "A Generic CAD Model for Arbitrarily Shaped and Multi-Layer Integrated Inductors on Silicon Substrates", to be presented at 1997 European Solid-State Circuits Conf., Southampton, UK.

[2] J. Macedo, M. Copeland, P. Schvan, "A 1.9GHz Silicon Receiver with On-chip Image Filtering", *IEEE 1997 CICC*, pp. 181-184.